Notice of Allowability	Application No.	Applicant(s)	
	10/790,381	LUKANC ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *after-final amendment filed 8/2/2007*.
2. ☒ The allowed claim(s) is/are *1-13 and 15-21*.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JACK CHIANG
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

Reasons For Allowance

1. The following is an examiner's statement of reasons for allowance:

Claims 1-13 and 15-21 are allowed because the prior art made of record does not teach or suggest a method of producing an integrated circuit device layout representation corresponding to an IC device design in the manner as recited in the claims.

2. With respect to claims 1-11, the prior art fails to teach the combination of steps in claim 1 including the following particular steps as recited in claim 1:

(e) modifying at least one of (i) portions of the layout representation which include structures demonstrating poor manufacturability and (ii) portions of the layout representation in which extra manufacturability margin is present;

wherein for portions of the layout representation including structures demonstrating poor manufacturability, step (e) includes:

at least one of (i) providing more space between adjacent structures, (ii) decreasing linewidth of one or more structures, and (iii) making edges of one or more structures wider.

3. With respect to claims 12-13 and 15-21, the prior art fails to teach the combination of steps in claim 12 including the following particular steps as recited in claim 12:

evaluating a scanning electron microscope (SEM) image of the selected exemplary layout portion printed on a wafer;

identifying areas on the SEM image that are problematic with respect to manufacturability; and

for each problematic area on the SEM image, locating the corresponding portion of the simulation image and determining acceptable ranges for the one or more metrics based on the simulation image.

4. With respect to claims 16-21, the prior art fails to teach the combination of steps in claim 16 including the following particular steps as recited in claim 16:

(e) modifying at least one of (i) portions of the layout representation which include structures demonstrating poor manufacturability and (ii) portions of the layout representation in which extra manufacturability margin is present;

wherein for portions of the layout representation in which extra manufacturability margin is present, step (e) includes:

at least one of (i) moving outer corners of structures closer to adjacent structures, (ii) moving contacts closer to inner corners of metal lines, (iii) moving contacts closer to polysilicon end caps, (iv) reshaping active or metal layers to maintain width and space, and (v) adding side extensions to polysilicon end caps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER